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Vertical-Tunneling Field-Effect Transistor Based on WSe_2-MoS_2 Heterostructure with Ion Gel Dielectric

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A p-type tunneling field-effect transistor is demonstrated based on a van der Waals vertical heterostructure of WSe_2 and MoS_2, utilizing the ion gel dielectric as top gate. Band-to-band tunneling is achieved by modulating the band alignment of the heterojunction of WSe_2 and MoS_2 with gating the WSe_2 channel through ion gel top gate. A fabricated tunneling field-effect transistor shows a minimum subthreshold swing of 36 mV dec^{-1} and ON/OFF current ratio of 10^6 at room temperature. Furthermore, evidence of band-to-band tunneling is clearly confirmed through temperature dependent *I–V* characteristics. This work holds considerable promise for the low-power computational devices based on integrated circuits.

Tunneling field-effect transistor (TFET) is one of the promising candidates for low-power switching devices in the digital logic application because it provides the possibility of obtaining a subthreshold swing (SS) less than the Boltzmann limit of 60 mV dec^{-1} at room temperature.[1] Different from the conventional metal-oxide-semiconductor field-effect transistor (MOSFET) which is based on the mechanism of thermionic emission at the source, TFET is governed by a band-to-band tunneling (BTBT) process that the Boltzmann distribution of carriers in the source is filtered by the energetic window between the valence band maximum (VBM) and the conduction band minimum (CBM).[1] For these reasons, TFETs with SS less than 60 mV dec^{-1} have been reported for various materials such as CNT,[2] Si,[3] and III–V[4] compound semiconductors. However, a sub-60 mV dec^{-1} over several decades of the drain current has been rarely demonstrated, and they usually have a low on current compared to MOSFET due to the limitation of the tunneling process.

Recently, two-dimensional (2D) semiconductors have attracted significant attention for TFET because of the good gate controllability and sharp band edges with ultrathin thickness.[5–12] In addition, 2D materials including graphene, hexagonal boron nitride (h-BN), and transition metal dichalcogenides (TMDCs) are free of dangling bond on their surface, making it possible to form clean interface of the 2D heterostructure without the lattice mismatching.[13–16] Hence, many TFETs using 2D materials, including black phosphorus (BP),[17] BP–MoS_2,[18–20] WSe_2–MoS_2,[21,22] WSe_2–$SnSe_2$,[23,24] WS_2–SnS_2,[25] $MoTe_2$–MoS_2,[26,27] HfS_2–MoS_2,[28] Ge–MoS_2,[29] and Si–MoS_2,[30] have been investigated. Although 2D semiconductors have their own advantages, few studies have achieved the SS less than 60 mV dec^{-1} because it is difficult to make good gate dielectric on the surface of 2D materials. Hence, a TFET based on the heterostructure of Ge and MoS_2 with a liquid ion gate has been able to achieve only the low SS of 31.1 mV dec^{-1} over several decades.[29]

In this work, we demonstrated a p-type TFET based on the heterostructure of WSe_2 and MoS_2 with ion gel (EMIM-TFSI) dielectric as top gate. The fabricated TFET shows the minimum SS of 36 mV dec^{-1} at room temperature and the ON/OFF current ratio of ≈10^6. In the previous studies of TFETs based on 2D semiconductors,[20–30] most results exhibit n-type characteristics. However, this is the first time a p-type TFET based on 2D–2D heterostructure with SS less than 60 mV dec^{-1} at room temperature is demonstrated. The heterostructure of WSe_2 and MoS_2 initially shows type II (staggered gap) band alignment. In order to realize the BTBT, high electric field at the heterostructure should be applied to form the type III (broken gap) band alignment. Hence, we have utilized the ion gel top gate dielectric, which has extremely high capacitance. Through the temperature dependent *I–V* measurement, we confirmed that the SS of p-type TFET is independent of the temperature, which is the evidence of BTBT.

Figure 1a shows the schematic diagram of a TFET based on the 2D–2D heterostructure of WSe_2 and MoS_2. The fabrication process is as follows. First, WSe_2 and MoS_2 flakes were exfoliated on 90 nm SiO_2/p++Si wafer, respectively. Then, heterostructures of WSe_2 and MoS_2 were made by the pick-up transfer process. Source contact to MoS_2 and drain contact to WSe_2 were patterned by the photolithography, followed by the deposition of the source with 10 nm Ti/40 nm Au and the drain with 10 nm Pd/40 nm Au using the thermal evaporation system, sequentially. After the lift-off process, ion gel gate dielectrics are spin-coated and patterned by the photolithography, covering the gate electrode as well as the channel. Here, ion gel is made from the mixture of EMIM ($C_6H_{11}N_2^+$):TFSI($C_2F_6NO_4S_2^-$), PEG-DA, and HOMPP with

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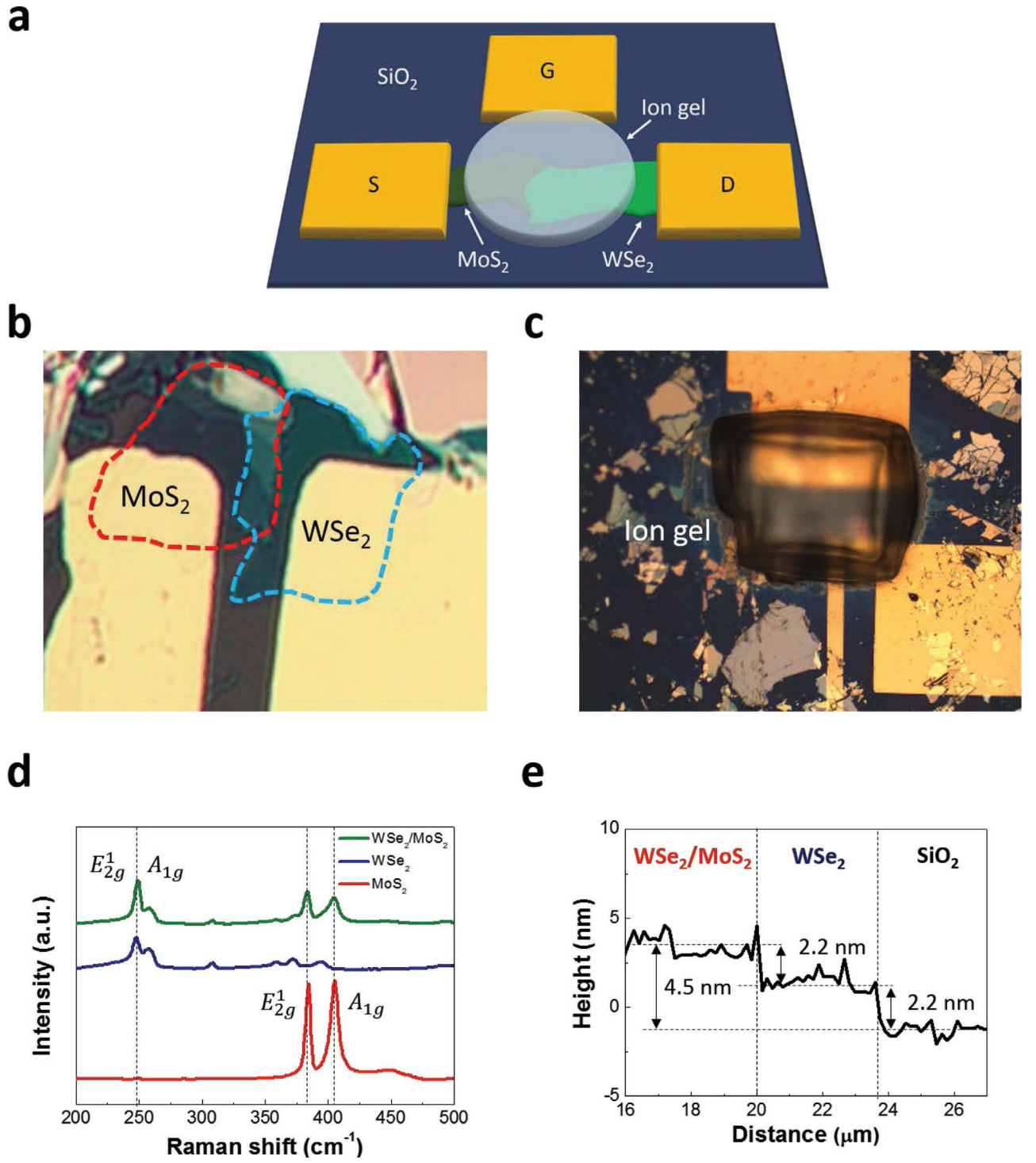

Figure 1. a) Schematic of a tunneling field-effect transistor (TFET) based on van der Waals heterostructrue of WSe_2 and MoS_2. b) Optical microscope image of the heterojunction of WSe_2 and MoS_2. c) Optical microscope image of the TFET after the deposition of the ion gel dielectric as top gate. d) Raman spectra of the heterojunction of WSe_2 and MoS_2, WSe_2, and MoS_2. e) AFM thickness profile of the heterojunction.

a weight ratio of 88:8:4. The structural formula and role of ionic liquid and polymers are shown in Figure S1 (Supporting Information). This ion gel gate dielectric has high capacitance, making it possible to induce strong electric field at the channel with small gate voltage. Figure 1b and c represent the optical microscopic image of the device before and after ion gel gate deposition, respectively. Raman spectrum of WSe_2 and MoS_2 shows the characteristic features as shown in Figure 1c. Vibrational peaks of the in-plane E^1_{2g} and out-of-plane A_{1g} were revealed for WSe_2 and MoS_2, respectively. Figure 1d shows the

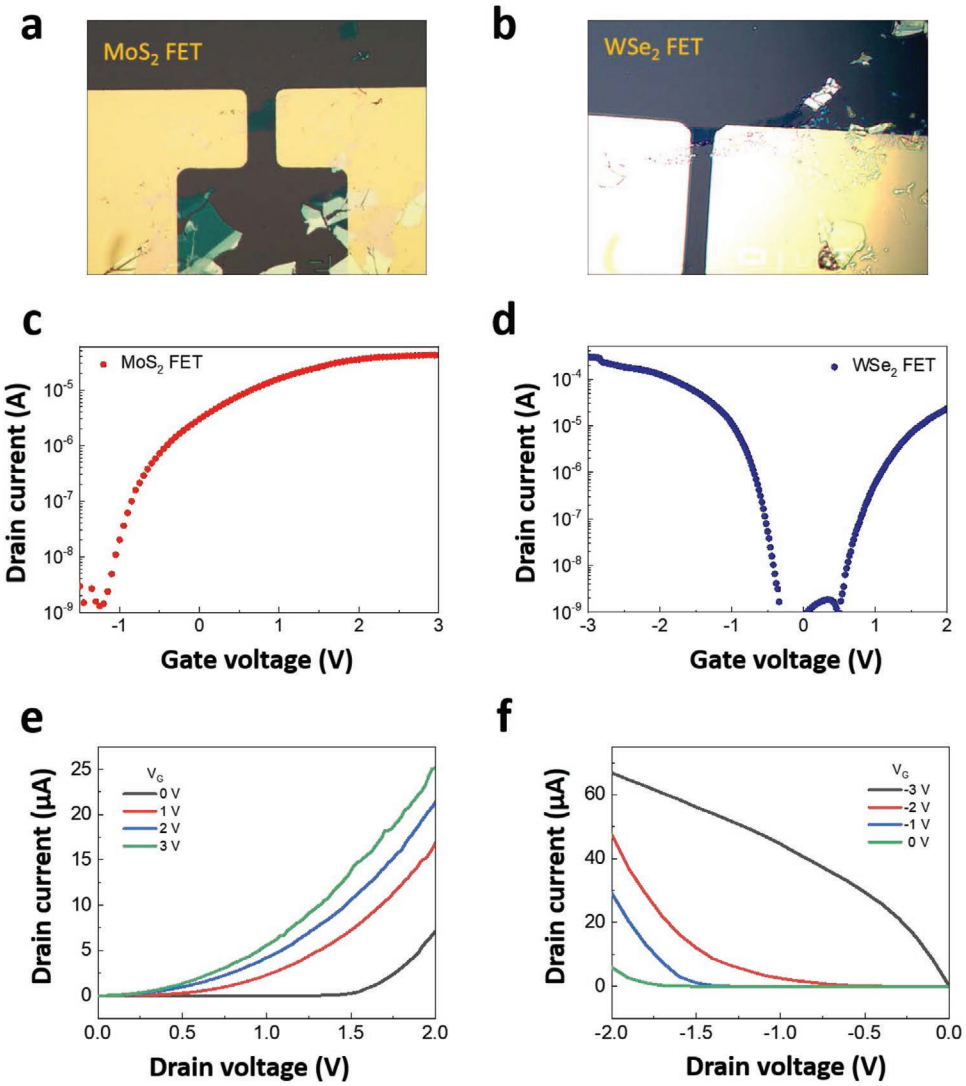

Figure 2. a,b) Optical microscope image of MoS_2 and WSe_2 FET before the deposition of the ion-gel dielectric. c,d) I_D–V_G transfer characteristics of MoS_2 and WSe_2 FET at a drain voltage of 1 V. e,f) I_D–V_D output characteristics of MoS_2 and WSe_2 FET.

atomic force microscopy (AFM) thickness profile of WSe_2 and MoS_2. It is considered that WSe_2 and MoS_2 are three layers.

Figure 2a,b presents the optical microscope image of the few-layer MoS_2 and WSe_2 FET before the deposition of an ion gel top gate. After the deposition of the ion gel top gate, we measured the I_D–V_G transfer and I_D–V_D output characteristics of the MoS_2 and WSe_2 FETs, as shown in Figures 2c–f. The source and drain electrodes for the MoS_2 and WSe_2 FETs were deposited by Ti/Au and Pd/Au, respectively. The contact resistances of the source and drain were measured as 1.3 and 20 kΩ, respectively, in Figure S2 (Supporting Information). MoS_2 FET with ion gel top gate shows general n-type I_D–V_G characteristics with ON/OFF current ratio over 10^4. On the other hand, WSe_2 ion gel FET exhibits ambipolar I_D–V_G characteristics with ON/OFF current ratio of 10^5 for p-type region and 10^4 for n-type region. We confirmed three regions of the hole transport region ($V_G < -1$ V), intrinsic region (-1 V $< V_G < 1$ V), and the electron transport region ($V_G > 1$ V). These results indicate that the ion gel top gate efficiently modulates the charge carrier density of the channel within small gate voltage. When the gate voltage is applied to this ion gel, positive ions ($EMIM^+$) and negative ion ($TFSI^-$) are adsorbed on the channel of MoS_2 and WSe_2 FET depending on the polarity of the gate voltage, forming an electronic double layer at the interface.

Figure 3a shows the I_D–V_G transfer characteristics of the TFET based on the heterostructure of WSe_2 and MoS_2 at different drain voltages at the room temperature. The gate leakage current is shown in Figure S3 (Supporting Information). We applied the reverse bias at the drain voltages, which has negative polarity, in order to induce the BTBT. When the V_G from -5 to -3 V is applied to the top gate, negative ions ($TFSI^-$) are adsorbed onto the surface of the channel, resulting in the accumulation of holes. The band structure of the heterojunction is changed from type II (staggered gap) to type III (broken gap). The band-to-band tunneling occurs at this region, and a minimum SS of 36 mV dec^{-1} is achieved. The drain current is suppressed at $V_G > -3$ V, because the tunneling process is cut off by the band gap. On the other hand, as the V_G increase to

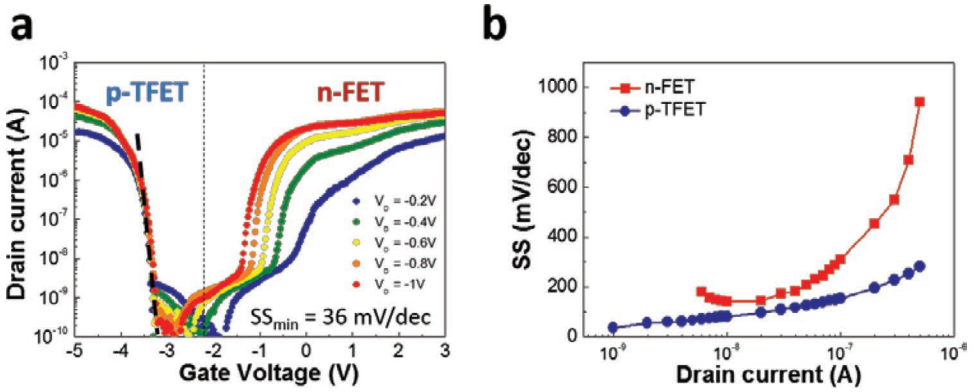

Figure 3. a) I_D–V_G transfer characteristics of the tunneling field-effect transistor (TFET) based on van der Waals heterostructure of WSe_2 and MoS_2 at different drain voltage. b) SS of the TFET as a function of the drain current.

positive voltage, positive ions ($EMIM^+$) are adsorbed onto the surface of the channel, inducing the accumulation of electrons. At this region, the device shows the typical n-type FET characteristics. The ON/OFF current ratio of p-TFET and n-FET region is over 10^6 with high ON current of 100 μA at the $V_D = -1$ V. The shoulder at the n-FET region from $V_G = -3$ to −1 V can be attributed to the Schottky barrier at the source and drain hindering the transport of carriers, as shown in Figure S4 (Supporting Information). In addition, we confirmed the hysteresis characteristics by measuring the dual sweep, as shown in Figure S5 (Supporting Information). Figure 3b shows the SS as a function of the drain current in the region of p-TFET and n-FET. The SS of p-TFET ($36 < SS < 300$ mV dec^{-1}) is less than n-FET ($180 < SS < 1000$ mV dec^{-1}) due to the BTBT process.

The semi-log plot of I_D–V_D output characteristics of the device are shown in **Figure 4**a. When the V_G is applied to −4 V, holes are accumulated in the WSe_2 and the heterojunction becomes p–N junction. Hence, in the case of the reverse bias in which V_D is negative voltage, the BTBT current flows through the energetic window between VBM of the WSe_2 and CBM of the MoS_2, while the forward bias that V_D is positive voltage lowers the energy band of WSe_2 and electrons of MoS_2 goes over the barrier as shown in Figure 4b. Typically, thermionic emission current is larger than BTBT because the BTBT current is limited in the energetic window. On the other hand, when V_G is applied to +2 V, electrons are accumulated in the WSe_2 and the heterojunction becomes n–N junction. Hence, in the case of the negative V_D, electrons in the WSe_2 goes to MoS_2 without the barrier while electrons of MoS_2 goes over the barrier in the positive V_D as shown in Figure 4b. Thus, the drain current at the negative V_D is larger than the positive V_D. When the V_G is applied to −2 V, the Fermi levels of WSe_2 is located in the middle of the band gap and the heterojunction is depleted. Hence, the drain current is suppressed in both negative and positive V_D. The energy band of the heterojunction of WSe_2 and MoS_2 was investigated in Figure S6 (Supporting Information). Figure 4c–e shows the energy band diagram for the reverse bias, small forward bias, and forward bias when the gate voltage is zero, respectively. When a reverse bias is applied to the device, the tunneling current is dominant because the tunneling width and height at the junction are lowered by the electric field between the source and drain. When a small forward bias is applied to the device, there is a tunneling current as well as drift and diffusion currents, but the tunneling current decreases as the tunneling width and height at the junction increase. When a forward bias is applied to the device, the drift and diffusion current are dominant. In our case, it is considered that the negative differential resistance (NDR) phenomenon was obscured by drift and diffusion current, which is enhanced by the thermal energy of the room temperature.

In order to confirm the evidence of the BTBT in the p-TFET region, we measured the temperature dependent I_D–V_G transfer characteristics as shown in **Figure 5**a. The gate voltage was applied from −5 to +3 V with the drain voltage of −1 V for the temperature range 180 to 300 K. When the gate voltage becomes below −3 V, the slope of this p-TFET region is independent of the temperature because of the BTBT. However, as the gate voltage increases over −3 V, the drain current at the intrinsic region ($-3\ V < V_G < +1$ V) and the slope of n-FET are clearly dependent on the temperature because the transport mechanism is based on the thermionic emission. Figure 5b shows a minimum and an average SS of p-TFET and n-FET region, respectively. The average SS was extracted for three decades change of the drain current. The SS of n-FET is much larger than 60 mV dec^{-1} and strongly dependent on the temperature, while p-TFET shows the weak dependence on the temperature below 60 mV dec^{-1}. This work exhibits sub-60 mV dec^{-1} of SS in the p-TFET based on 2D–2D heterostructure. The performance comparison of TFET based on 2D materials is shown in Figure S7 (Supporting Information). Although the confirmation of the negative differential resistance (NDR) phenomenon was not performed, it has been already investigated in previous reports of the Esaki diode based on the WSe_2–MoS_2 heterostructure.[16] Therefore, we have focused on the demonstration of subthermionic p-TFET based on 2D–2D heterostructure in this study.

In conclusion, a p-type TFET based on van der Waals heterostructure WSe_2–MoS_2, using the ion gel as top gate, is demonstrated with a minimum SS of 36 mV dec^{-1} at the room temperature for the first time. The band structure of the heterojunction of WSe_2–MoS_2 initially shows type-II (staggered gap) alignment. The ion gel dielectric with high capacitance allows the energy band modulation from type II to type III (broken gap), resulting in the BTBT that provides steep SS as well as high ON/OFF current ratio of 10^6. In addition, we confirmed

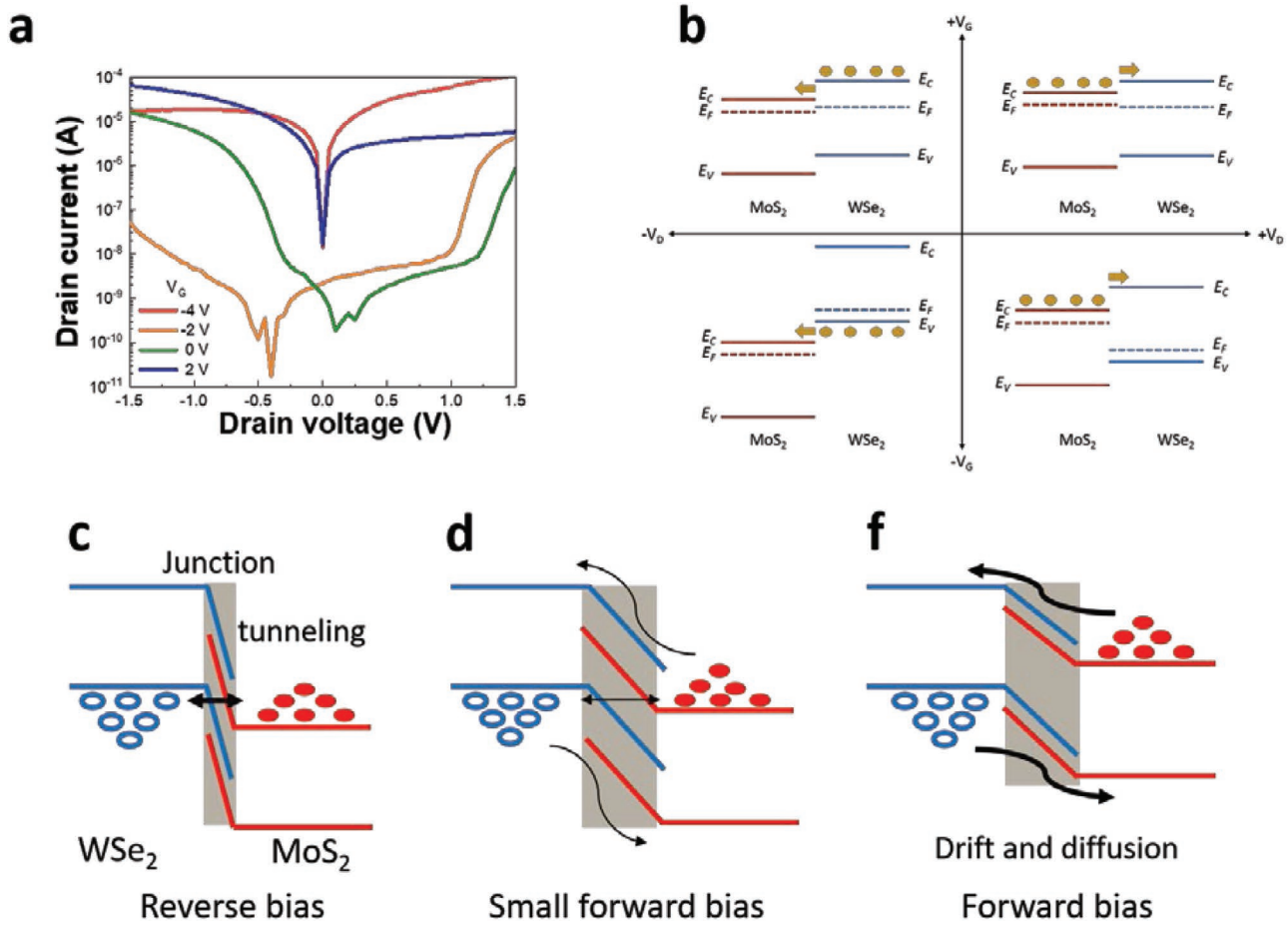

Figure 4. a) Semi-log plot of the I_D–V_D output characteristics of the tunneling field-effect transistor (TFET). b) Energy band diagram of the TFET at different voltages of the drain and gate. The energy band diagram of the device for the reverse bias c), small forward bias d), and forward bias e) when the gate bias is zero.

the evidence of BTBT through temperature dependent I_D–V_G transfer characteristics. This work represents the possibility of the integration of n-type as well as p-type 2D-2D TFET, which could further reduce the power consumption, similar to the complementary metal-oxide-semiconductor (CMOS).

Experimental Section

The electrical measurements were conducted using a semiconductor parameter analyzer (4200 SCS, Keithley Instruments) and probe station (MS-TECH). All measurements were performed in ambient conditions.

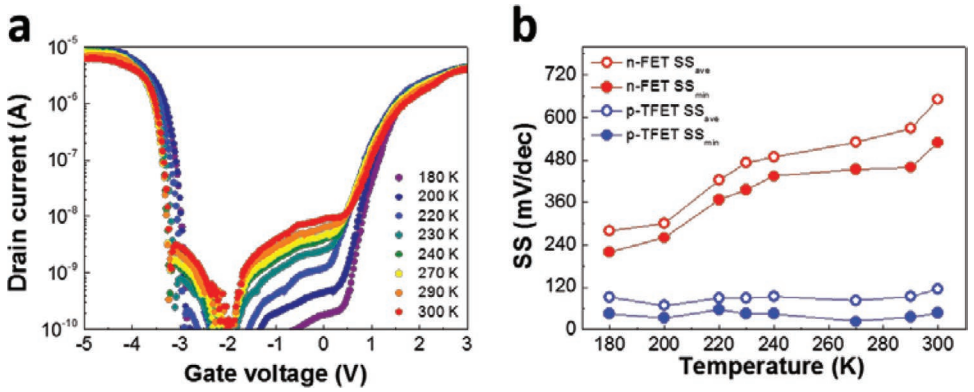

Figure 5. a) Temperature dependent I_D–V_G transfer characteristics of the tunneling field-effect transistor (TFET) from 180 to 300 K. b) A minimum and an average SS of the n-FET and p-TFET as a function of the temperature. The average SS was extracted for the three decades change of the drain current.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

heterostructures, ion gel dielectrics, MoS_2, tunneling transistors, WSe_2

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[1] A. M. Ionescu, H. Riel, *Nature* **2011**, *479*, 329.
[2] J. Appenzeller, Y. M. Lin, J. Knoch, P. Avouris, *Phys. Rev. Lett.* **2004**, *93*, 196805.
[3] W. Y. Choi, B. Park, J. D. Lee, T. K. Liu, *IEEE Electron Device Lett.* **2007**, *28*, 743.
[4] B. Ganjipour, J. Wallentin, M. T. Borgström, L. Samuelson, C. Thelander, *ACS Nano* **2012**, *6*, 3109.
[5] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, M. S. Strano, *Nat. Nanotechnol.* **2012**, *7*, 699.
[6] G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D. Neumaier, A. Seabaugh, S. K. Banerjee, L. Colombo, *Nat. Nanotechnol.* **2014**, *9*, 768.
[7] F. Xia, H. Wang, D. Xiao, M. Dubey, A. Ramasubramaniam, *Nat. Photonics* **2014**, *8*, 899.
[8] A. Castellanos-Gomez, *Nat. Photonics* **2016**, *10*, 202.
[9] A. K. Geim, I. V. Grigorieva, *Nature* **2013**, *499*, 419.
[10] D. Jariwala, T. J. Marks, M. C. Hersam, *Nat. Mater.* **2017**, *16*, 170.
[11] X. Wang, F. Xia, *Nat. Mater.* **2015**, *14*, 264.
[12] K. S. Novoselov, A. Mishchenko, A. Carvalho, A. H. Castro Neto, *Science* **2016**, *353*, aac9439.
[13] T. Roy, M. Tosun, J. S. Kang, A. B. Sachid, S. B. Desai, M. Hettick, C. C. Hu, A. Javey, *ACS Nano* **2014**, *8*, 6259.
[14] Y. Gong, J. Lin, X. Wang, G. Shi, S. Lei, Z. Lin, X. Zou, G. Ye, R. Vajtai, B. I. Yakobson, H. Terrones, M. Terrones, B. K. Tay, J. Lou, S. T. Pantelides, Z. Liu, W. Zhou, P. M. Ajayan, *Nat. Mater.* **2014**, *13*, 1135.
[15] A. Nourbakhsh, A. Zubair, M. S. Dresselhaus, T. Palacios, *Nano Lett.* **2016**, *16*, 1359.
[16] T. Roy, M. Tosun, X. Cao, H. Fang, D.-H. Lien, P. Zhao, Y.-Z. Chen, Y.-L. Chueh, J. Guo, A. Javey, *ACS Nano* **2015**, *9*, 2071.
[17] P. Wu, J. Appenzeller, *IEEE Electron Device Lett.* **2019**, *40*, 981.
[18] J. Xu, J. Jia, S. Lai, J. Ju, S. Lee, *Appl. Phys. Lett.* **2017**, *110*, 033103.
[19] X. Jiang, X. Shi, M. Zhang, Y. Wang, Z. Gu, L. Chen, H. Zhu, K. Zhang, Q. Sun, D. W. Zhang, *ACS Appl. Nano Mater.* **2019**.
[20] S.-H. Yang, Y.-T. Yao, Y. Xu, C.-Y. Lin, Y.-M. Chang, Y.-W. Suen, H. Sun, C.-H. Lien, W. Li, Y.-F. Lin, *Nanotechnology* **2019**, *30*, 105201.
[21] C. Li, X. Yan, X. Song, W. Bao, S. Ding, D. W. Zhang, P. Zhou, *Nanotechnology* **2017**, *28*, 415201.
[22] J. He, N. Fang, K. Nakamura, K. Ueno, T. Taniguchi, K. Watanabe, K. Nagashio, *Adv. Electron. Mater.* **2018**, *4*, 1800207.
[23] T. Roy, M. Tosun, M. Hettick, G. H. Ahn, C. Hu, A. Javey, *Appl. Phys. Lett.* **2016**, *108*, 083111.
[24] X. Yan, C. Liu, C. Li, W. Bao, S. Ding, D. W. Zhang, P. Zhou, *Small* **2017**, *13*, 1701478.
[25] J. Wang, R. Jia, Q. Huang, C. Pan, J. Zhu, H. Wang, C. Chen, Y. Zhang, Y. Yang, H. Song, F. Miao, R. Huang, *Sci. Rep.* **2018**, *8*, 17755.
[26] B. Koo, G. H. Shin, H. Park, H. Kim, S.-Y. Choi, *J. Phys. D: Appl. Phys.* **2018**, *51*, 475101.
[27] Y. Balaji, Q. Smets, C. J. L. D. L. Rosa, A. K. A. Lu, D. Chiappe, T. Agarwal, D. H. C. Lin, C. Huyghebaert, I. Radu, D. Mocuta, G. Groeseneken, *IEEE J. Electron Devices Soc.* **2018**, *6*, 1048.
[28] W. Zhang, T. Kanazawa, Y. Miyamoto, *Appl. Phys. Express* **2019**, *12*, 065005.
[29] D. Sarkar, X. Xie, W. Liu, W. Cao, J. Kang, Y. Gong, S. Kraemer, P. M. Ajayan, K. Banerjee, *Nature* **2015**, *526*, 91.
[30] G. H. Shin, B. Koo, H. Park, Y. Woo, J. E. Lee, S.-Y. Choi, *ACS Appl. Mater. Interfaces.* **2018**, *10*, 40212.

